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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/653,295	08/31/2000	Allen Yen	3-6-16	4287

7590 01/28/2002

Docket Administrator (Room 3C-512)
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EXAMINER
NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/28/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/653,295	Applicant(s) YEN ET AL.	
	Examiner Cuong Q Nguyen	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) *7-10* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restriction

1. Applicant's election with traverse of Group I, claims 1-6 in Paper No. 5 is acknowledged. The traversal is on the ground(s) that the removal of the etching step does not imply that the claimed process would be enabled by means other process. This is not found persuasive because referring to the restriction requirement set forth in the Office Action paper no.7, it clearly shows that the alternative method proposed by the examiner would be distinct from the process claimed such that selectively forming conductive layers at desired areas instead of forming the conductive layers and the remove the unwanted portions of conductive layers by etching step. It was clearly established that group I and II inventions are in fact distinct in Paper No.4.

The requirement is still deemed proper and is therefore made FINAL.

Oath/Declaration

2. The oath/declaration filed on 08/31/00 is acceptable.

Specification

3. This application does not contain an abstract of the disclosure as required by 37 CFR 1.72(b). An abstract on a separate sheet is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai et al. (US 5,643,804) in view of Watanabe et al. (US 5,481,490).

Regarding claims 1-3, Arai et al. discloses a semiconductor device comprising: a first interconnect level (the level of layer 102); a second interconnect level (the level of layer 107); a third interconnect level (the level of layer 108); a stack of alternating conductive and insulative layers formed in vertical alignment with respect to an underlying plane, wherein the stack layers formed between the first and second interconnect levels and including a first conductive layer, a first insulator layer on the first conductive layer, a second conductive layer on the first insulative layer, a second insulative layer on the second conductive layer, and a third conductive layer on the second insulative layer with the first and third conductive layer commonly connected through the first , second and third interconnect levels. See Arai et al.'s Fig.9(A-D).

Arai et al. , as shown in Fig.3, teaches that the first interconnect level (102) is an out electrode of a thin film integrated circuit which includes a semiconductor layer (303) having a source region (306) and a drain region (309), source/drain electrodes (308).

however, Arai et al. does not explicitly teach that the out put electrode (102) connect to semiconductor layer (303).

It is well known in the art and also taught by Watanabe et al. that the capacitor structure is commonly connected to a semiconductor layer such as source/drain region of the FET transistor in order to control the charge storage in the capacitor structure by ON/OFF states of the FET transistor.

Therefore, it would have ben obvious to one of ordinary skill in the art connecting the output electrode (102) to the semiconductor source/drain layer through the source/drain electrodes (308) in Arai et al.'s device.

Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arai et al. in view of Watanabe et al. and further in view of Saia et al. (US 5,736,448).

Arai et al. and Watanabe et al. teach all the limitations of claims 1-3 as shown above but fails to teach that the stack comprises five conductive layers configured to provided four capacitor connected in parallel.

It is conventional and also taught by Saia et al. (Fig.9) that a stack capacitor structure comprises five conductive layers configured to provided four capacitor connected in parallel. is commonly formed in the integrated circuit in order to increase the capacitance of the capacitor structure.

Therefore, it would have been obvious to one of ordinary skill in the art to incorporate the stack capacitor as taught by Saia et al. in order to increase the capacitance of the capacitor structure.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arai et al. in view of Watanabe et al. and further in view of Roy (US 6,180,976).

Arai et al. and Watanabe et al. teach all the limitations of claims 1-3 as shown above and further teaches that the first interconnect level including a via portion and a trench portions of a Damascene structure and the third interconnect level including a second via portion. Arai et al. and Watanabe et al. fails to teach that the third interconnect level including a trench portions of a Damascene structure.

Roy discloses a capacitor structure comprises a multi-level of interconnections connected to a capacitor structure and the multilevel of interconnection can be formed of a single or dual damascene interconnection structure. See Roy's Fig.10, Fig.13 and col.4 lines 1-7.

Roy clearly established that it is conventional to form the interconnection by a single or dual damascene interconnection structure. Therefore, it would have been obvious to one of ordinary skill in the art to form the third interconnect level of the device formed by the combination of Arai et al. and Watanabe et al. of dual damascene structure instead of single damascene structure.

Conclusion

5. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

6. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

January 24, 2002